✉: renjithsphd@gmail.com
: +91-9446777732
github: github.com/renjithsasikumar
ORCiD: 0000-0003-2971-1992

Renjith S

LinkedIn: renjith sasikumar

Education

Indian Institute of Technology Palakkad — Palakkad, India
Ph.D. in Electrical Engineering — 2018–2023

- **Coursework from Indian Institute of Technology Madras**
- **Supervisor:** Dr. Revathy Padmanabhan
- **Relevant courses:** Fundamentals of Semiconductor Devices, Nanoelectronic Devices, MOS Device Modeling and Characterization, Computational Methods for Electrical Engineering
- **Thesis title:** "Transport in resistive switching devices"

Rajiv Gandhi Institute of Technology Kottayam — Kottayam, India
Master of Technology in Advanced communication and information systems — 2011–2013

- **Best thesis award winner**
- **Supervisors:** Prof. Anish Babu K K and Dr. Leena Mary
- **Relevant courses:** Linear Algebra, Advanced Digital Signal Processing, Real-Time and Embedded systems

College of Engineering Poonjar — Kottayam, India
Bachelor of Technology in Electronics and Communication Engineering — 2003–2007

Skills Summary

- **Characterization:** **Semiconductor parameter analyzer, DC probe station**, RF probe station, and X-ray diffraction: *(acquired during my Ph.D. by characterizing resistive switching devices, MOS capacitors)*
- **Modeling:** Numerical techniques, **Finite difference method** (*Used for simulation of diode, both equilibrium and non-equilibrium characteristics: as part of Teaching assistance, IIT Palakkad*)
- **Software:** **MATLAB** *(used for automated analysis of device characteristics and numerical modeling of devices: as part of Ph.D. and Teaching assistant)*, **Easy-Expert** *(used for automated characterization of resistive switching devices)*, LT-spice, **Cadence-Virtuoso** *(used for simulation of memristors, its crossbar arrays, using proposed Verilog-A models)*
- **Programming:** **Verilog** *(acquired during my Ph.D., for Teaching assistance in Digital electronics and Computer organization Labs)* , **Verilog-A** *(used for modeling of memristive devices, during Ph.D.)*, **Python** *(for analytical process modeling (oxidation) and device modeling (MOS capacitor), as part of Teaching, and for feature extraction from speech signal, during my masters project)*, **Embedded C** *(used for programming of AVR micro-controller based embedded system design for banking automation)*
- **Fabrication:** Adhered to clean room protocols and procedures, DC and RF Sputtering equipment, Mask aligner, Wire bonder (acquired during my Ph.D. and research assistant jobs in IIT Palakkad) .
- **Design:** CMOS circuit design *(acquired during my Ph.D., for Teaching assistance in Digital electronics and Computer organization Labs)*

Relevant Research Work

- **Oxide-based resistive switching (memristor) devices** ***(manuscript under preparation)***
  - In collaboration with Tokyo electron Ltd., Japan, who fabricated the devices.
  - ***Characterized*** HfO_2 and $HfZrO_2$-based memristors and ***analyzed*** their transport mechanisms.
  - ***Modeled*** various transport mechanisms using Verilog-A to explain its I-V characteristics and ***synaptic plasticity***. ***Simulated*** various switching characteristics in Cadence-Virtuoso, using proposed models.
- **2D material-based ECM memristor devices [3] [4] [5]**
  - ***Modeled*** the transport using MATLAB and Verilog-A to explain its I-V characteristics, associated variability, and ***synaptic plasticity***. ***Simulated*** various switching characteristics.

- **Neural network using memristor crossbar arrays** ***(manuscript under preparation)***
  - ***Designed*** a memristor-based neural network for pattern classification.
  - ***Analyzed*** the system's performance using the memristor models and estimated ***device variability's*** impact.

Experience

Indian Institute of Technology Palakkad Palakkad, India
Research Assistant January 2023–ongoing

- Micro/Nano fabrication clean rooms: Fabrication and process optimization of MOS devices, resistive switching devices in Class 10000 and Class 1 lakh clean room environments using specialized equipment such as thermal evaporator, sputtering systems and mask aligner.
- Electrical characterization: conducting DC measurements, temperature dependent I-V and C-V measurements, and stressed I-V measurements on fabricated devices

Indian Institute of Technology Palakkad Palakkad, India
Teaching Assistant January 2018–December 2022

- Laboratories handled: Digital electronics Lab, Electrical workshop, Computer organization and architecture lab.
- Courses assisted: Solid state devices, Nanoelectronics, Digital electronics.

Vidya Academy of Science and Technology-Technical campus Thiruvananthapuram, India
Assistant Professor June 2015–December 2017

- Responsibilities: Academic coordinator, Lab in charge (Digital signal processing), Staff advisor
- Courses taught: Digital electronics, Signals and systems, Computer organization and architecture, VLSI design, Electromagnetic theory.

College of Engineering Thiruvananthapuram Thiruvananthapuram, India
Assistant Professor (ad-hoc) December 2013–April 2015

- Courses taught: Computer organization and architecture, Analog electronics, Nanoelectronics, and Basics of electronics engineering.

ADSP Research lab, RIT Kottayam Kottayam, India
Project Assistant June 2013–December 2013

- Responsibilities: Design and development of various speaker recognition and speech recognition systems

College of Engineering Thiruvananthapuram Thiruvananthapuram, India
Lecturer (ad-hoc) July 2010–May 2011

- Courses taught: Basics of electronics engineering, Solid state devices, and Electronics circuits

Aminod integrated technologies (former Gensole Integrated Technologies) Thiruvananthapuram, India
Embedded Engineer and co-founder June 2013–December 2017

- Responsibilities: Design and development of banking automation devices.

Certifications

- **Advanced Training Program on Nanofabrication and Characterization techniques in MOS Capacitance module**
  - Conducted at ***Center for Nano-Science and Engineering, Indian Institute of Science, Bangalore***
  - Supported by, ***the Ministry of Education (former, MHRD), India***
  - 03^{rd}December 2019 - 13^{th}December 2019
- **Two-week training program on CMOS, Mixed Signal and Radio Frequency VLSI Design**
  - Conducted at ***Indian Institute of Technology, Kharagpur***
  - Supported by, ***the Ministry of Education (former, MHRD), India***
  - 30^{th}January 2017 - 04^{th}February 2017

Publications

[1] **R. Sasikumar**, K. L. Ganapathi, D. Misra, and R. Padmanabhan, "Modeling of variability-aware memristive neural networks", in *Proc. 2023 Device Research Conference (DRC)*, doi:10.1109/DRC58590.2023.10187082, Jun. 2023, pp. 1–2.

[2] **R. Sasikumar** and R. Padmanabhan, "Variability-aware electrochemical metallization based memristive neural network for pattern classification", in *Proc. 18th Conf. Ph.D Research in Microelectron. and Electronics (PRIME)*, doi:10.1109/PRIME58259.2023.10161791, Jun. 2023, pp. 253–256.

[3] **R. Sasikumar**, A. Ajoy, and R. Padmanabhan, "Modeling of electrochemical metallization-based two-dimensional material memristors for neuromorphic applications", *IEEE Trans. Nanotechnol.*, vol. 20, pp. 912–921, Dec. 2021, doi:10.1109/TNANO.2021.3133356.

[4] **R. Sasikumar**, A. Ajoy, and R. Padmanabhan, "Modeling of electrochemical metallization-based transport in vertical transition metal dichalcogenide (TMD) memristors", in *Proc. IEEE 20th Int. Conf. Nanotechnol. (IEEE-NANO)*, doi:10.1109/NANO47656.2020.9183542, Jul. 2020, pp. 159–163.

[5] **R. Sasikumar** and R. Padmanabhan, "Modeling the dynamics of switching in electrochemical metallization (ECM)-based memristors", in *Proc. 5th Int. Conf. Emerg. Electronics (IEEE ICEE 2020)*, doi:10.1109/ICEE50728.2020.9777032, Nov. 2020, pp. 1–4.

[6] **R. Sasikumar**, A. Joseph, and A. B. K.K., "Isolated digit recognition for malayalam- an application perspective", in *Proc. Int. Conf. on Control Commun. and Computing (ICCC)*, doi:10.1109/ICCC.2013.6731648, Dec. 2013, pp. 190–193.

[7] **R. Sasikumar**, L. Mary, A. B. K.K., A. Joseph, and G. M. George, "Prosody-based voice forgery detection using svm", in *Proc. Int. Conf. on Control Commun. and Computing (ICCC)*, doi:10.1109/ICCC.2013.6731711, Dec. 2013, pp. 527–530.

Manuscripts under preparation/revision

[1] **R. Sasikumar**, A. Ajoy, and R. Padmanabhan, "Two-dimensional filament growth model for ECM based memristors," *manuscript under preparation.*

[2] **R. Sasikumar**, K. L. Ganapathi, D. Misra and R. Padmanabhan, "Modeling of synaptic plasticity in oxide-based valence change memristors for neuromorphic applications," *manuscript under preparation.*

[3] **R. Sasikumar**, K. L. Ganapathi, D. Misra and R. Padmanabhan, "Design of variability aware memristor crossbar neural network for pattern classification applications," *manuscript under preparation.*

Awards and fellowships

- Best M.Tech. Thesis award winner, contest conducted by Center for Engineering Research and Development (CERD), Kerala state
- Half Time Research Assistantship (HTRA), funded by the Ministry of Education (former, MHRD), India, during the Ph.D. research
- Post Graduate Scholarship by All India Council for Technical Education (AICTE) during the Master's Programme

Declaration: I declare that all information in this resume is true and correct to the best of my knowledge and belief

Renjith S